This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A driver circuit for a liquid crystal panel, comprising:

a gate driving unit for applying signal voltages to gate lines of a liquid crystal panel;

a data driving unit for applying signal voltages to data lines of a liquid crystal panel;

a switching unit for transferring power to the data and gate driving units;

a timing controller for generating timing signals to drive the liquid crystal panel depending upon horizontal and vertical synchronization signals which are input from an outside; and

a determination unit for determining whether either one of or both of the horizontal and vertical synchronization signals are input from the outside, and controlling the switching unit and the timing controller, and performing a normal mode or powersaving mode depending upon determination results.

2. (Original) The driver circuit as set forth in claim 1, wherein the determination unit outputs a Power Down Control (PDC) signal to the switching unit unless one of the horizontal and vertical synchronization signals is input.

3. (Original) The driver circuit as set forth in claim 1, wherein the determination unit outputs a PDC signal to the switching unit unless both of the horizontal and vertical synchronization signals are input.

4. (Original) The driver circuit as set forth in claim 1, wherein the determination unit further determines whether the horizontal or vertical synchronization signals are normal.

5. (Original) The driver circuit as set forth in claim 4, wherein the determination unit determines whether the horizontal or vertical synchronization signals are normal by checking periods of the horizontal or vertical synchronization signals or counting numbers of clocks in a specified range.

6. (Original) The driver circuit as set forth in claim 4, wherein the determination unit outputs a PDC signal to the switching unit if the horizontal or vertical synchronization signals are abnormal.

7. (Original) The driver circuit as set forth in claim 1, wherein the switching unit is a Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET).

8. (Previously Presented) The driver circuit as set forth in claim 2, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.

9. (Original) The driver circuit as set forth in claim 1, further comprising a Transmission Minimized Differential Signaling (TMDS) reception unit for decoding a TMDS data signal input from an outside to a horizontal or vertical synchronization signal and a digital image signal and outputting the decoded horizontal or vertical synchronization signal and the decoded digital image signal.

10. (Canceled)

11. (Previously Presented) The driver circuit as set forth in claim 1, wherein the timing controller holds the timing signal until the horizontal or vertical synchronization signal becomes normal.

12. (Previously Presented) A liquid crystal display comprising:
a backlight having a light source;

a liquid crystal panel on which a plurality of thin film transistors are formed on intersections of a plurality of data and gate lines; and

a driver circuit for driving the liquid crystal panel, the driver circuit comprising:

a gate driving unit for applying signal voltages to gate lines of a liquid crystal panel;

a data driving unit for applying signal voltages to data lines of a liquid crystal panel;

a switching unit for transferring power to the data and gate driving units;

a timing controller for generating timing signals to drive the liquid crystal panel depending upon horizontal and vertical synchronization signals which are input from an outside; and

a determination unit for determining whether either one of or both of the horizontal and vertical synchronization signals are input from the outside, and controlling the switching unit and the timing controller, and performing a normal mode or powersaving mode depending upon determination results.

13. (Original) The liquid crystal display as set forth in claim 12, wherein the determination unit outputs a PDC signal to the switching unit unless one of the horizontal and vertical synchronization signals is input.

14. (Original) The liquid crystal display as set forth in claim 12, wherein the determination unit outputs a PDC signal to the switching unit unless both of the horizontal and vertical synchronization signals are input.

15. (Original) The liquid crystal display as set forth in claim 12, wherein the determination unit further determines whether the horizontal or vertical synchronization signals are normal.

16. (Original) The liquid crystal display as set forth in claim 15, wherein the determination unit determines whether the horizontal or vertical synchronization signals

are normal by checking periods of the horizontal or vertical synchronization signals or counting numbers of clocks in specified ranges.

17. (Original) The liquid crystal display as set forth in claim 15, wherein the determination unit outputs a PDC signal to the switching unit if the horizontal or vertical synchronization signals are abnormal.

18. (Original) The liquid crystal display as set forth in claim 12, wherein the switching unit is a MOSFET.

19. (Previously Presented) The liquid crystal display as set forth in claim 13, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.

20. (Original) The liquid crystal display as set forth in claim 12, further comprising a TMDS reception unit for decoding a TMDS data signal input from an outside to a horizontal or vertical synchronization signal and a digital image signal and outputting the decoded horizontal or vertical synchronization signal and the decoded digital image signal.

21. (Canceled)

22. (Previously Presented) The liquid crystal display as set forth in claim 12, wherein the timing controller holds the timing signal until the horizontal or vertical synchronization signal becomes normal.

23. (Previously Presented) The driver circuit as set forth in claim 3, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.

24. (Previously Presented) The driver circuit as set forth in claim 6, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.

25. (Previously Presented) The liquid crystal display as set forth in claim 14, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.

26. (Previously Presented) The liquid crystal display as set forth in claim 17, wherein the switching unit shuts off power to the data driving unit and the gate driving unit when the PDC signal is input from the determination unit.